Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claim in the application:

Listing of Claims:

1. (currently amended) A method for forming contact openings between bit line patterns, the method comprising the steps of:

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a) forming bit line patterns on a substrate including word line patterns, thereby forming a first resulting structure;

b) forming an interlayer insulating layer on the first resulting structure;

c) etching the interlayer insulating layer with an etching mask defining a straight line shape, and forming a straight line shaped contact opening between neighboring bit line patterns; and

d) forming insulating layers on sidewalls of the bit line patterns only exposed through the contact opening.

2. (original) The method of claim 1, wherein the interlayer insulating layer is formed of a material having a dielectric constant less than 3.5.

3. (original) The method of claim 2, wherein in step b), the interlayer insulating layer is formed of an oxide layer.

4. (original) The method of claim 3, where in step c), the interlayer insulating layer is etched with a gas mixture including Ar, C, and F.

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5. (original) The method of claim 4, wherein in step c), the interlayer insulating layer is etched at a pressure of 1 mTorr to 100 mTorr.

6. (previously presented) A method of claim 1, wherein top surfaces of the bit line patterns are covered with a layer selected from a group consisting of a silicon nitride layer, a silicon oxynitride layer, and an oxide layer.

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7. (original) The method of claim 2, wherein in step b), the interlayer insulating layer is formed of a polymer.

8. (previously presented) The method of claim 7, wherein in step c), the interlayer insulating layer is etched by using a gas selected from a group consisting of Ar, O_2, N_2, H_2, CH_4, C_2H_4, and C_xF_y.

9. (original) The method of claim 8, wherein in step c), the interlayer insulating layer is etched at a pressure of 1 mTorr to 100 mTorr.

Claims 10-20 (canceled)

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